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10/825,189	04/15/2004	Ravi Kumar Arimilli	AUS920040002US1	7640

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EXAMINER	
SAVLA, ARPAN P	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 06/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,189	ARIMILLI ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *15 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 13-22* is/are rejected.

7)☒ Claim(s) *2-7,10-12 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/825,189 has a total of 22 claims pending in the application, there are 3 independent claims and 19 dependent claims, all of which are ready for examination by Examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

INFORMATION CONCERNING DRAWINGS

Drawings

2. Applicant's drawings submitted September 7, 2004 are acceptable for examination purposes.

OBJECTIONS

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "System And Method For Completing Updates To Entire Cache Lines With Address-Only Bus Operations."

4. In the section entitled "Related Application" Applicant must properly identify the co-pending applications with its corresponding application number, which is "10/825,188."

Appropriate corrections required.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 2-7 and 17-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. **As per claim 2**, the claim limitation "to determining" in line 5 is vague and indefinite. Applicant may consider amending the claim read "to determine."

8. **Also per claim 2**, the claim recites the limitation "the STQ controller" in line 7. There is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending the claim to read "a STQ controller."

9. **As per claim 3**, the claim limitation "a STQ controller" in line 1 is vague and indefinite. It is unclear whether this "STQ controller" is the same as the "STQ controller" from claim 2 or an entirely new "STQ controller." For the purposes of examining the instant application the Examiner will interpret it as the same "STQ controller" from claim 2.

10. **As per claim 17**, the claim limitation "when a store queue entry selected for dispatch by an provides a complete update" in lines 4-5 is vague and indefinite. For the purposes of examining the instant application the Examiner will interpret the limitation to read "when a store queue entry selected for dispatch by an RC mechanism provides a complete update" because that will provide sufficient antecedent basis for the limitation "said RC mechanism" in line 7.

11. **Also per claim 17**, the claim limitation "said RC mechanism assigned said update" is vague and indefinite. For the purposes of examining the instant application the Examiner will interpret the limitation to read "said RC mechanism assigned to complete said update" because that logically follows from the previous limitation in claim 17.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1, 8-9, 13-17, and 21-22 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's "Description of the Related Art" appearing in Applicant's specification, hereafter referred to as "Applicant's admitted prior art" in view of Gregor (U.S. Patent 5,023,776).

14. **As per claim 1**, Applicant's admitted prior art discloses in a data processing system having multiple processors each having a processor core, store queue (STQ) mechanism, RC mechanism, and associated processor cache, a method for facilitating cache line updates responsive to processor-issued store operations (paragraph 0003, lines 6-8; paragraph 0004; Fig. 2). *It should be noted that "L2 cache" is analogous to "associated processor cache."*

Applicant's admitted prior art does not expressly disclose determining when a store queue entry selected for dispatch by an RC machine provides an update to an entire cache line;

and completing said update to said entire cache line with address-only operations, wherein no data tenure is requested when an entire cache line is being overwritten.

Gregor discloses determining when a store queue entry selected for dispatch by an RC machine provides an update to an entire cache line (col. 43, line 58 – col. 44, line 2; col. 45, lines 11-19); *It should be noted that "L2 cache write buffer" is analogous to "store queue entry", "L2 cache control" is analogous to "RC mechanism", and "full line write" is analogous to "update to an entire cache line." It should also be noted that "the receipt of end-of-operation for the instruction executing the sequential stores" determines when the L2 cache write buffers are written to the L2 cache.*

and completing said update to said entire cache line with address-only operations, wherein no data tenure is requested when an entire cache line is being overwritten (col. 45, lines 16-19). *It should be noted that the L2 cache control uses just*

*"address bits 25 and 26" to accomplish the full line write and does **not** load the cache line being overwritten, therefore, no data tenure is requested.*

Applicant's admitted prior art and Gregor are analogous art because they are from the same field of endeavor, that being hierarchical caching.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Gregor's write buffers and cache control within Applicant's admitted prior art's data processing system.

The motivation for doing so would have been to include a system of write buffers to be used in conjunction with the novel store queues for increasing the capacity of the store queues so that the various processors of the multiprocessor system may not be inhibited in their operation when attempting a store operation to the shared L2 cache and to main memory (Gregor, col. 2, lines 18-24).

Therefore, it would have been obvious to combine Applicant's admitted prior art and Gregor for the benefit of obtaining the invention as specified in claim 1.

15. **As per claim 8**, the combination of Applicant's admitted prior art/Gregor disclose following a miss at said processor cache or a hit at said processor cache with a cache line that becomes stale prior to completion of said update (Gregor, col. 33, lines 26-28), *It should be noted that "modified" is analogous to "stale."*

said completing step comprises:

issuing an address-only operation to obtain write permission for said cache line (Gregor, col. 33, lines 60-63);

and automatically updating said cache line with data from said entry once said write permission is obtained (Gregor, col. 33, lines 26-30 and 60-63).

16. **As per claim 9**, Applicant's admitted prior discloses a processor chip for utilization within a data processing system having a memory hierarchy, said processor chip comprising:

a processor core (paragraph 0004, lines 2-3; Fig. 2, element 203);

a store queue having multiple entries, each entry including registers for storing address and data of store operations issued by the processor core and byte-enable bits, one for each smallest storage granule of data that may be stored by a store operation (paragraph 0004, lines 2-3; paragraph 0005; Fig. 2, elements 207, 209, 211, 213, 215, and 217);

a store queue (STQ) controller that monitors and controls said store queue (paragraph 0004, lines 2-4; Fig. 2, element 205);

arbitration logic associated with said STQ controller that selects an entry from among multiple eligible entries available for dispatch to be stored in a lower level cache (paragraph 0004, lines 2-5; paragraph 0006, lines 1-3; Fig. 2, element 206);

and an RC mechanism that perform updates to cache lines within said lower level cache utilizing data from the entry selected for dispatch (paragraph 0004, lines 5-7; Fig. 2, element 221).

Applicant's admitted prior art does not expressly disclose first logic for determining when all storage granules within a store queue entry have received data from said processor core before said entry is selected for dispatch;

and second logic within an RC machine of said RC mechanism assigned to update a target cache line with data of said entry for completing said update of the target cache line without initiating a data tenure on the system bus, wherein said update is completed regardless of whether said cache line is present in said lower level cache or said cache line data is stale.

Gregor discloses first logic for determining when all storage granules within a store queue entry have received data from said processor core before said entry is selected for dispatch (col. 43, line 58 – col. 44, line 2); *It should be noted that "L2 cache write buffer" is analogous to "store queue entry" and "L2 control 26k" is analogous to "first logic." It should be noted that "the receipt of end-of-operation for the instruction executing the sequential stores" implies all the L2 write buffers have received data from the processor.*

and second logic within an RC machine of said RC mechanism assigned to update a target cache line with data of said entry for completing said update of the target cache line without initiating a data tenure on the system bus, wherein said update is completed regardless of whether said cache line is present in said lower level cache or said cache line data is stale (col. 45, lines 11-19). *It should be noted that "L2 cache control" is analogous to "second logic." It should also be noted that the L2 cache control does* ***not*** *load the cache line being overwritten, therefore, no data tenure is requested.*

Please see the 103 rejection of claim 1 above for the reasons to combine Applicant's admitted prior art and Gregor.

17. **As per claims 13 and 21**, the combination of Applicant's admitted prior art/Gregor disclose said second logic comprises:

means for determining whether the targeted cache line is within said processor cache (Applicant's admitted prior art, paragraph 0018, lines 3-4; Fig. 3C, element 333); *It should be noted that paragraph 0058, lines 3-6 define this means as an "RC machine."*

means, when said targeted cache line is within said processor cache, for issuing an address only operation to a system bus requesting write permission for said cache line (Applicant's admitted prior art, paragraph 0020, lines 3-6; Fig. 3C, element 337); *It should be noted that paragraph 0058, lines 6-10 define this means as an "RC machine."*

and when said targeted cache line is not within said processor cache and said entire cache line is being updated:

means for issuing an address-only operation on said system bus to obtain write permission and invalidate all other copies of said cache line within other processor caches (Gregor, col. 33, lines 60-63 and 47-51); *It should be noted that paragraph 0046 and paragraph 0058 define this means as the an "RC machine." It should also be noted that "to manipulate address bits 25 and 27 to permit the L2 cache line accesses" is analogous to issuing an address-only operation on a system bus to obtain write permission."*

and means for writing said address and data to a line within said processor cache (Gregor, col. 33, lines 26-28). *It should be noted that paragraph 0059, lines 11-13 define this means as an "RC machine."*

18. **As per claim 14**, the combination of Applicant's admitted prior art/Gregor disclose means for tagging said targeted cache line with a most recently modified coherency state following said update (Gregor, col. 12, lines 2-5). *It should be noted that paragraph 0046, lines 9-12 define this means as "RC machine logic." Gregor's "L2 control" is equivalent to Applicant's "RC machine logic." It should also be noted that the "status array" is analogous to "tagging said targeted cache line with a most recently modified coherency state."*

19. **As per claim 15**, the combination of Applicant's admitted prior art/Gregor disclose when said entry is not a full entry, said RC machine further comprises:

means for obtaining a copy of said cache line data when said cache line data is not present within said processor cache (Applicant's admitted prior art, paragraph 0019, lines 3-5; paragraph 0022, lines 1-4); *It should be noted that paragraph 0060, lines 1-2 of Applicant's specification appear to define this means as an "RC machine."*

and means for obtaining write permission for said cache line when said write permission is not currently owned by said processor cache, wherein said update is completed only when said cache line data is present in said cache and write permission for the cache line is obtained (Applicant's admitted prior art, paragraph 0022, lines 1-3; paragraph 0023. *It should be noted that paragraph 0041, lines 3-6 of Applicant's specification appear to define this means as a "processor."*

20. **As per claim 16**, Applicant's admitted prior art discloses a data processing system comprising:

a processor chip having a processor core, store queue (STQ) mechanism, RC mechanism, and associated processor cache (paragraph 0003, lines 6-8; paragraph 0004; Fig. 2);

a memory hierarchy coupled to said processor chip and providing coherent memory operation (paragraph 0003, lines 6-8).

Applicant's admitted prior art does not expressly disclose means for completing updates to a cache line of the processor cache with data from processor-issued stores, wherein when all storage granules of said cache line are being updated by a single RC machine tenure, the update is completed without requiring a data tenure on the system bus, regardless of whether the cache line being updated is present in the processor cache or the cache line is present but contains stale data.

Gregor discloses means for completing updates to a cache line of the processor cache with data from processor-issued stores, wherein when all storage granules of said cache line are being updated by a single RC machine tenure, the update is completed without requiring a data tenure on the system bus, regardless of whether the cache line being updated is present in the processor cache or the cache line is present but contains stale data (col. 45, lines 11-19). *It should be noted that paragraph 0049, lines 3-5 of Applicant's specification appear to define this means as "additional logic components." Gregor's "L2 cache control" is equivalent to Applicant's "additional logic components." It should also be noted that the L2 cache control does* ***not*** *load the cache line being overwritten, therefore, no data tenure is requested.*

Please see the 103 rejection of claim 1 above for the reasons to combine Applicant's admitted prior art and Gregor.

21. **As per claim 17**, the combination of Applicant's admitted prior art/Gregor discloses said store queue mechanism comprises a store queue that includes a plurality of entries, each entry having at least a data and address register and byte-enable bits (Applicant's admitted prior art, paragraph 0004, lines 2-3; paragraph 0005; Fig. 2, elements 207, 209, 211, 213, 215, and 217).

said processor chip further includes first logic for determining when a store queue entry selected for dispatch by an RC mechanism provides a complete update to a target cache line of the processor cache (Gregor, col. 43, line 58.– col. 44, line 2; col. 45, lines 11-19); *It should be noted that "L2 cache write buffer" is analogous to "store queue entry", "L2 control 26k" is analogous to "first logic", "L2 cache control" is analogous to "RC mechanism" and "full line write" is analogous to "complete update to a target cache line." It should also be noted "the receipt of end-of-operation for the instruction executing the sequential stores" determines when the L2 cache write buffers are written to the L2 cache.*

and said RC mechanism assigned to complete said update includes second logic for completing said update to said target cache line with address-only operations, wherein no data tenure is requested when the target entire cache line is being completely updated (Gregor, col. 45, lines 16-19). *It should be noted that the L2 cache control uses just "address bits 25 and 26" to accomplish the full line write and does* ***not*** *load the cache line being overwritten, therefore, no data tenure is requested.*

22. **As per claim 22**, the combination of Applicant's admitted prior art/Gregor disclose when said entry is not a full entry, said RC mechanism further comprises:

means for obtaining a copy of said cache line data when said cache line data is not present within said processor cache (Applicant's admitted prior art, paragraph 0019, lines 3-5; paragraph 0022, lines 1-4); *It should be noted that paragraph 0060, lines 1-2 of Applicant's specification appear to define this means as an "RC machine."*

and means for obtaining write permission for said cache line when said write permission is not currently owned by said processor cache, wherein said update is completed only when said cache line data is present in said cache and write permission for the cache line is obtained (Applicant's admitted prior art, paragraph 0022, lines 1-3; paragraph 0023. *It should be noted that paragraph 0041, lines 3-6 of Applicant's specification appear to define this means as a "processor."*

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

Allowable Subject Matter

23. **Claims 2-7, 10-12, and 18-20** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-7 and 18-20 also need to be rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

24. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose the combination including the limitations of:

(**Claim 2**) "...logically ANDing each of the byte enable bits of the store queue entry to determine when all storage granules of said store queue entry have been updated; and providing a full signal to a STQ controller when said logically ANDing step indicates all storage granules of said entry have been updated."

(**Claims 10 and 18**) "...a series of AND logic associated with each of said entries that receives as input a value of each of said byte-enable bits and provides a single AND output that indicated when all said byte-enable bits are set, indicating a full entry."

(**Claim 11**) "...means for logically ANDing a value of each bit within said byte enabled register corresponding to said target cache line to generate an AND output; means for providing said AND output to said STQ controller; means, when said AND output indicates all bits have been set, for said STQ queue controller to mark said entry as eligible for dispatch."

(**Claim 19**) "...means for logically ANDing a value of each bit within said byte enabled register corresponding to said target cache line to generate an AND output; and means for providing said AND output to a STQ controller of the store queue mechanism."

25. As dependent **claims 3-7, 12, and 20** depend from an allowable base claim; they are at least allowable for the same reasons as noted above.

26. If Applicant should choose to rewrite the independent claims to include the limitations recited in either one of **claims 2, 10-11, and 19**, the Applicant is encouraged to amend the title of the invention such that it is descriptive of the invention as claimed as required by sec. 606.01 of the MPEP. Furthermore, the Summary of the Invention and the Abstract should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of sec. 1302.01 of the MPEP.

27. As allowable subject matter has been indicated, Applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the MPEP.

Claims Rejected in the Application

Per the instant office action, **claims 1, 8-9, 13-17, and 21-22** have received a first action on the merits and are subject of a first action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 6,557,084 (Freerksen et al.) discloses an apparatus and method to improve performance of reads from and writes to shared memory locations.

2. U.S. Patent 6,678,799 (Ang) discloses aggregation of cache-updates in a multi-processor, shared-memory system.

3. U.S. Patent 6,772,298 (Khare et al.) discloses a method and apparatus for invalidating a cache line without data return in a multi-node architecture.

4. U.S. Patent Application Publication 2004/0064643 (Jamil et al.) discloses a method and apparatus for optimizing line writes in cache coherent systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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June 6, 2006

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